Journal of Universal Computer Science, vol. 18, no. 7 (2012), 899-900
submitted: 20/3/12, accepted: 28/3/12, appeared: 1/4/12 © J.UCS

Adaptive Methodologies and Designs for Network-on-Chip based Systems

J.UCS Special Issue

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Network-on-Chip (NoC) is an emerging paradigm for communications within large VLSI systems implemented on a single silicon chip. IT is used as a new approach to designing complex System-on-a-chip (SoCs) design. NoC-based systems can accommodate multiple complex SoC designs. In a NoC-based system, modules such as processor cores, memories and specialized IP blocks exchange data using a on-chip network. A NoC is constructed from multiple point-to-point data links interconnected by switches also called routers, such that messages can be relayed from any source module to any destination module over several links, by making routing decisions at the switches. VLSI designers of embedded systems face several problems, among which we can cite, for instance, planning the architecture that is most suitable to a given application is order to improve performance and mapping the sub-systems that form the application into the available platform infra-structure. Evolutionary computation can be used as a very robust tool to bring some answers to this kind of design problems.

This special issue of Universal Journal of Computer Science covers hardware, middleware and application designs and synthesis tools that exploit the evolutionary computation principles and other innovative computing paradigms to provide CAD tools for embedded systems in general and NoC-based systems in particular. The issue presents three papers whose main contributions are described in the sequel.

In the first contribution, which is entitled “Mapping and Scheduling in Heterogeneous NoC through Population-Based Incremental Learning”, Freddy Bolanos, Jose Edison Aedo, Fredy Rivera and Nader Bagherzadeh address the problem of mapping and scheduling, which takes advantage of a Population-Based Incremental Learning (PBIL) algorithm. The simulation results suggest that the PBIL approach is able to find optimal mapping and scheduling, in a multi-objective fashion. A 2-D heterogeneous mesh was used as target architecture for implementation. The

PBIL representation is also suited to deal with more complex architectures, such as 3-D meshes.

In the second contribution, which is entitled "ACO-based algorithms for search and optimization of routes in NoC platform", Luneque Silva Jr, Nadia Nedjah and Luiza de Macedo Mourelle propose using ant colony algorithms to find and optimize routes in a mesh-based NoC. The routing optimization is driven by the minimization of total latency in packets transmission. The simulation results show the effectiveness of the ant colony inspired routing by comparing it with general-purpose algorithms for deadlock free routing under different traffic patterns.

In the third contribution, which is entitled "Designing Robust Routing Algorithms and Mapping Cores in Networks-on-Chip: A Multi-objective Evolutionary-based Approach", Maurizio Palesi, Rafael Tornero, Juan Manuel Orduña, Vincenzo Catania and Daniela Panno present a new strategy that simultaneously refines the mapping and the routing function to determine the Pareto optimal configurations which optimize average communication delay and routing robustness. The proposed strategy has been applied on both synthetic and real traffic scenarios. The obtained results show how the solutions found by the proposed approach outperforms those provided by other approaches proposed in literature, in terms of both performance and fault tolerance.

As guest editors of this special issue of J.UCS, we wish to thank all the authors for their hard work and their promptness. Also, our special thanks go to the reviewers that provided us with the right feedback at the right time. This allowed us to fulfill our aim with the expected quality and delays.

Rio de Janeiro, March, 2012