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The Architecture and Circuital Implementation Scheme of a New Cell Neural Network for Analog Signal Processing

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Abstract: It is a difficult problem that using cellular neural network to make up of analog signal processing circuit. This paper presented the architecture of new cellular neural network SCCNN for analog signal processing circuits, designed the neural cell circuit, and developed the evolutionary design method of the SCCNN based on self-adapting genetic algorithm. In the architecture of new cellular neural network SCCNN, each neural cell connects with four neighborhood neural cells, the neural cell circuit and signal transfer line between neural cells are controlled by programmable switches. The validity of the SCCNN architecture and the evolutionary design method are verified through digital simulation. The experimental results indicate that the SCCNN hardware is a universal cellular neural network for analog signal processing circuit, which can be used to make up of the analog signal amplifier, analog signal filter, digit logic circuit, DAC circuit and so on.

Key Words: Cellular neural network, Evolutionary design, Analog signal processing circuit, DAC circuit

Category: B.7.3, B.2.3, C.5.4

1 Introduction

The artificial neural networks can be realized in two ways: hardware realization and software realization .Software realization of the artificial neural networks have the advantages that it is flexible and does not need the specific hardware, but its speed is low, and it is hard to be used in many real time fields. So hardware realization of the artificial neural networks is the unique effective approach to make the artificial neural networks useful for high speed computing [Wang and Cao 2006]-[Shuai and Feng et al. 2004].

The Hopfield Neural Network (HNN) and Cellular Neural Network (CNN) are widely used in image processing, pattern recognition, combination optimization, associate memory and intelligent control. But the HNN has many problems, for example, parasitic state, local minimum and undetermined parameter of the HNN. Although there have already been many improved methods about the HNN in order to overcome these problems, a universal method has not been developed. The CNN is a regular space structure consisted by a mass of same cells, every neural cell of the CNN has a continuous cell state and can only

connect with its adjacent neural cells. The CNN can overcome some defects of the HNN, and can be easily realized by VLSI hardware [Robert 2003]-[Keymeulen et al. 2004].

Analog hardware of the cell neural network has the advantage of fast speed and simple circuit, now it is used successfully in image processing and pattern recognition field. However using the cell neural network to design analog signals processing circuit is lack of research. For analog signal processing applications, this paper develops the universal architecture and circuit implementation of the analog cell neural network, the experiment results prove the feasibility of the new analog cell neural network.

2 The Architecture of the Cellular Neural Network

The hardware architecture of the new Switch-Controlled Cellular Neural Network (SCCNN) is made of MN 2-dimensional arrays that N, M may be 8, 16 and 32, as shown in Figure 1, M=N=4. All neural cells are the same in the circuit, the two neural cells are connected by 6 programmable control switches, and every neural cell can be addressed and re-programmed independently.

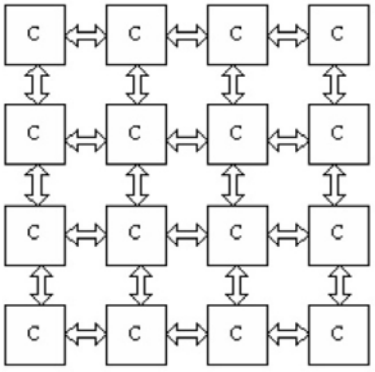

Figure 1: Architecture of the SCCNN hardware

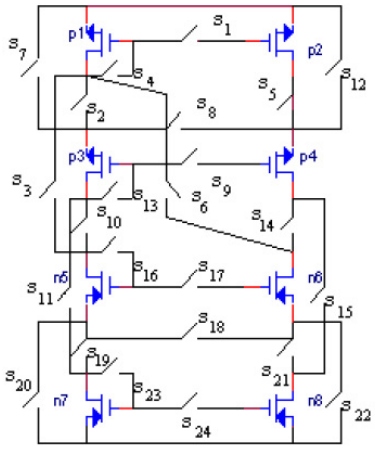

Figure 2: Schematic circuit of the neural cell

Figure 2 shows the schematic circuit of single neural cell in the SCCNN. The neural cell consists of 8 transistors and 24 programmable switches. The ON/OFF status of the switches S1-S24 determines the circuit topology and

functions of the neural cell. P1P4 are PMOS transistors, N5N8 are NMOS transistors. The switches S1-S24 are made of CMOS transistor, the ON/OFF status of the switches is defined by the configuration data of SCCNN, data "1" can be assigned to switch turned ON and "0" turned OFF.

Compared with traditional cellular neural network, the SCCNN circuit is very simple, there is no need for the DAC (Digital/analog converter) circuit and multiplier within the neural cells, and the neural cell also has the ability of fault tolerance.

3 Evolutionary Design Method of the SCCNN

With the characteristics of SCCNN, the evolutionary design method is used for designing the analog signal processing circuits of SCCNN. The key technologies are as follows.

3.1 The Coding Way of the SCCNN Circuit

Switches in the neural cell of the SCCNN are coded directly with the binary bit-string. Every switch is programmed by a bit of the bit-string. So the chromosome bit-string represents the control signal of all switches in the SCCNN, such as "1011", where, by convention we can assign "1" to switch turned ON and "0" to switch turned OFF. The length of bit-string for each neural cell of SCCNN in Figure 2 is 24, and there are 2200 bits in the SCNN's chromosome which includes these switch bits of the connecting line between neighborhood neural cells.

3.2 Individual Evaluation and Test of the SCCNN Circuit

Individual chromosome in evolutionary design of the SCCNN circuit is evaluated and tested by means of the Pspice simulation software. The individual chromosome is transformed to the circuit description text that can be recognized by the Pspice software, then the circuit defined by the chromosome is simulated in the Pspice software, and the fitness of the SCCNN circuit is calculated with the output response of the circuit. The input testing signal and the fitness function are determined according to the different circuit function.

3.3 Evolutionary Algorithm for Design of the SCCNN Circuit

The evolutionary algorithm is used to find the anticipant SCCNN circuit that achieves the performance index. The time consumed in testing and evaluating the SCCNN circuit is much longer than it consumed in the calculation of the evolution operator, so the generation scale of the evolution should be as small as

possible. So the mixed evolutionary mechanism that combines analog annealing algorithm and traditional evolutionary algorithm is developed. The main idea of the mixed evolutionary mechanism is that the evolution operation has only mutation and without crossover.

The evolutionary design process of the SCCNN is shown below.

(1) Generate a initial chromosome randomly.

(2) Evaluate the fitness of the individual SCCNN circuit.

The SCCNN circuit is determined by the chromosome bit-string. The circuit performance is analyzed by the Pspice software, and the fitness of the SCCNN circuit can be calculated according to corresponding fitness function.

(3) Judge if the ending condition of the evolution process is satisfied?

The evolution process of designing SCCNN circuit can be ended, when the ending condition is achieved, or it will go on. Here, the ending condition is that the fitness value of the individual circuit achieved a pre-fixed value, or the maximum generation of evolution is achieved.

(4) Design the evolutionary operator.

The evolutionary operation of the chromosome is done, and a new chromosome is generated. The mutation operation occurs at several bits of the chromosome randomly according to the individual fitness. The number of the bit g_m to mutate in the chromosome is determined by the formula (1) below.

$$g_m = g \times w_{m\max} \times \frac{(F_{it\max} - F_{it})}{F_{it\max}} \tag{1}$$

g is the length of the chromosome,$w_{m\max}$ is the maximal mutation rate, $F_{it\max}$ is the pre-fixed value of the maximal fitness, F_{it} is current fitness.

(5) Evaluate the fitness of new SCCNN circuit.

(6) Judge if new chromosome is better?

If the fitness value of new chromosome is better than old one, the old one is replaced by new chromosome, and the evolution design process go to (3). Otherwise, this mutation operation is cancelled, and the evolution design process jump to (4). And so on.

4 Example and Results

4.1 Design of the SCCNN Analog Amplifier

Taking the analog amplifier for the SCCNN application example, we analyze the test methods and the fitness function formation of the SCCNN circuit.

(I) Design objective: Adopt two neural cells to build up analog amplifier whose magnification is 10. The power VDD of analog amplifier is equal to 3.3V.

(II) Test method of the SCCNN circuit: Choose sine signal (u_i) as the input test stimuli of the SCCNN circuit. Suppose the input signal's amplitude is 10

mV, the signal frequency is 1kHz, the sin signal initial phase is 0, and the initial state of the circuit is 0. Thus the output response of the objective circuit is $u_o = -100 \times \sin(2\pi \cdot 1000t)$ (mV).

(III) The formation of fitness function: The fitness function reflects the similar degree of the output response between the actual circuit and the objective circuit of the SCCNN. The fitness function is designed as formula (2).

$$F_{it} = \frac{1}{\sqrt{\frac{1}{N-1} \cdot \sum_{i=1}^{N} [u'_o(i) - u_o(i)]^2}} \tag{2}$$

where, u'_o is the output voltage of the actual SCCNN circuit, and is the output voltage of the objective circuit. The data length of sampling signal is $N = 500$.

(1) Simulation results

The operator parameters of the evolution algorithm are set as follows: the maximum mutation rate is 0.06, the maximum fitness is 40, and the final generation is 5000. Among the total 50 statistical experiments of the SCCNN circuit design, the evolution algorithm converges 43 times, and the fitness value of the optimal individual circuit is 26.36, and the average convergence generation is 847. If the magnification time of the SCCNN analog amplifier is not equal to 10 ± 0.1 , the evolution process would appear no-converge. As evolution process is reset again, continuous two no-convergence phenomena have not occurred.

The SCCNN analog amplifier circuit is shown in Figure 3, and the output response of this SCCNN circuit is shown in Figure 4. Figure 5 shows a typical convergent state of the evolution process.

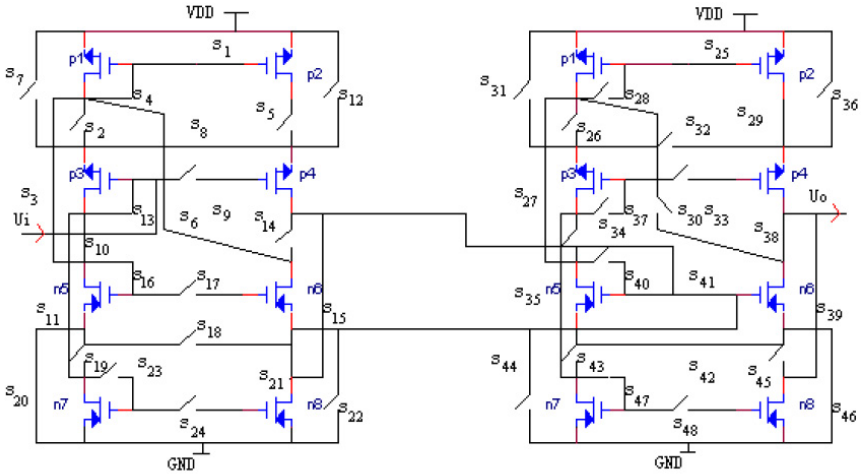

Figure 3: The SCCNN analog amplifier circuit

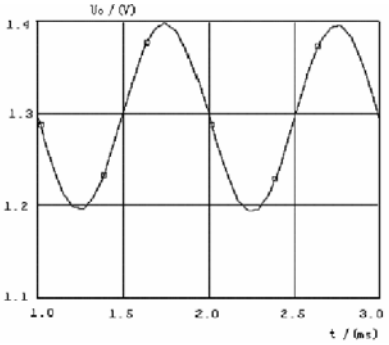

Figure 4: The output voltage response of the SCCNN analog amplifier

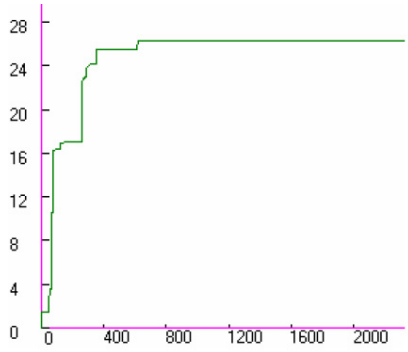

Figure 5: The fitness change of typical individual circuit in the SCCNN evolutionary design process

(2) Selection of the operator parameter of evolution algorithm

The influence of the operator parameter to SCCNN circuit design is shown in Table 1. The convergence rate is the percent ratio of convergent times to total evolution times. The time of statistical experiments is 20, and the maximum fitness is 80. From the Table 1, the better convergence rate is obtained when the maximum mutation rate is closed between 0.06–0.10. If the mutation rate is too low, the convergence speed of evolution process will be very slow. If the final generation is equal to 10000, the convergence success rate is improved. However, if the mutation rate is too high, the search process is close to a random search, thus induced a fast convergence speed but a low convergence rate.

Table 1: the influence of the operator parameter to the SCCNN circuit evolutionary design

Maximum mutation rate	Convergence rate	Optimal fitness	Average fitness	Average convergence generation
0.04	0.31	13.10	11.20	4615
0. 06	0.83	41.35	18.12	1253
0.10	0.72	18.50	12.25	1122

(3) The evaluation of the fitness of the SCCNN circuit

With the results of the SCCNN evolutionary design, one can concluded that the minority SCCNN circuits that are represented by the chromosomes what cannot accord with the convergence standard has better output voltage signal wave ,and the multiple of amplifier is close to the desired value. At the same time, in the SCCNN circuit which is represented by some convergent chromosome, the

output signal waves are distorted. Thus, the SCCNN circuit of the evolutionary design could not satisfy the characteristic demand of the analog amplifier.

The above reason can be found that the distributed capacity in the SCCNN neural cell circuit results on the difference of phase in the output response between the actual circuit and the target circuit. The different value of the phase which is not large affects the fitness evaluation. If the target output signal is $u_o = \sin(t)(V)$ and the actual output is $u'_o = \sin(t+\pi/36)(V)$, the phase difference between the two output signals is only 5 degrees. But the root mean square error between the two output signals is 6.17×10^{-2} (100 samples/per period). The root mean square error between the two output signals affects the function of fitness accord to formula (2). So, the phase difference between the two output signals affects the fitness function. To remove the affection, the individual fitness is evaluated after the maximum of the output response signal should be adjusted to 1.

The evaluation on the fitness of the SCCNN circuit chromosome is very important. The good method of evaluating SCCNN circuit could increase the success rate of evolution and improve the precision of circuit output response. In the application, the good way to evaluate the SCCNN circuit should be decided by designing the approach to test the circuit quickly, and to evaluate the fitness easily, according to the function of the desired circuit. For example, the analog band-pass filter is designed with the SCCNN, the fitness function can be constructed based on the frequency response of the SCCNN filter circuit.

4.2 Design of the SCCNN DAC Circuit

This experimental example aims at the evolution of 4-bit DAC circuit with the SCCNN. Four neural cells shown in Figure 6 are used, there are 108 programmable switches in Figure 6 are used, and the length of the chromosome is 108 bits. Figure 6 illustrates the connection between neural cells, IN0, IN1, IN2, IN3 are four-bit digital input signals, and the OUT is the output signal of the SCCNN circuit. The power VDD of DAC circuit is equal to 3.3V.

The input signal IN0, IN1, IN2, IN3 are rectangle signal whose amplitude is 3.3v, as shown in Figure 7.

The output voltage signal of the 4-bit DAC circuit is sampled at the middle time of each stage. There are 16 different stages in 4-bit DAC, compared the actual output with the ideal output, the fitness value is calculated with formula (2).The total sample points is N=16 in the testing of 4-bit DAC circuit. The output response of the SCCNN DAC circuit is shown in Figure 8.

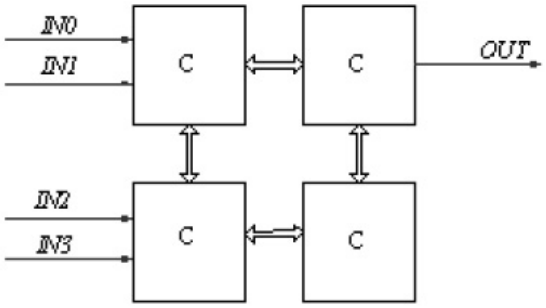

Figure 6: the SCCNN four cells used for the 4-bit DAC circuit

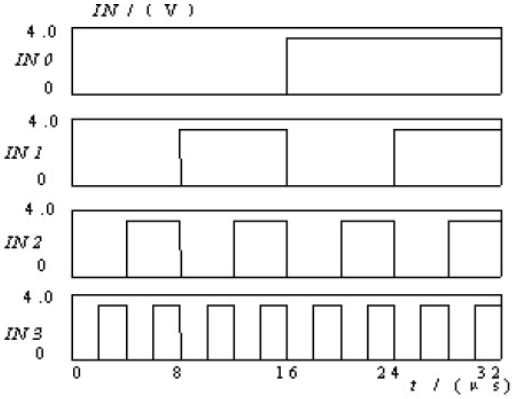

Figure 7: sequence chart of digital input signal in the SCCNN 4-bit DAC circuit

5 Conclusions

Through analysis of the experimental results above, the conclusions can be obtained as follows:

(1) The hardware circuit of the SCCNN is simple, and can be used to build up general analog signal processing circuit and DAC circuit.

(2) The evolutionary design method of the SCCNN is effective, and the improved evolutionary algorithm has high convergence rate.

(3) The test method of the SCCNN circuit and the design of the fitness function can influence the success rate of the SCCNN circuit evolutionary design.

The SCCNN hardware can not only realize the analog signal amplifier, analog filter circuits, half-wave rectifying circuits, non-linear compensating amplifiers,

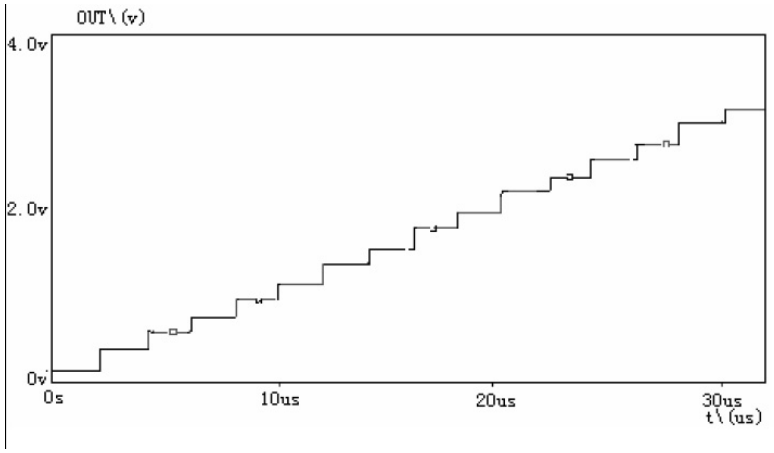

Figure 8: Output signal wave of the best SCCNN 4-bit DAC circuit

different digital logic circuits, and so on, but also can realize the self-adapting and self-repairing of these circuit inside neural cell.

The future works include that the optimization design of the SCCNN neural cell circuit is performed, and the SCCNN ADC (Analog to Digital Converter) circuit and analog multiplier are designed by evolutionary method.

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