

## Co-evolution for Communication: An EHW Approach

**Yasser Baleghi Damavandi, Karim Mohammadi**

(Iran University of Science and Technology, Iran  
yasser\_baleghi@iust.ac.ir, Mohammadi@iust.ac.ir)

**Abstract:** Evolvable Hardware (EHW) is a new concept that aims the application of evolutionary algorithms to hardware design. EHW can adapt itself to unknown environment based on features of the reconfigurable hardware. This paper presents outlines of the idea of using some EHW agents in a distributed system. These agents need to set up a self-organized communication to achieve the predesigned goal. The experiment that is demonstrated during the presentation, is to distribute a serial adder into two EHW parts, where good results has been shown in a co-evolutionary process.

**Key Words:** Evolvable hardware, Co-evolution, Genetic algorithm, Emergent communication

**Category:** I.1.2, I.2.3

### 1 Introduction

In the new bio-inspired approach of hardware developers, the evolution of a system is being preferred instead of the ever-increasing complicated process of design. However an important stage of hardware system design/evolution is the communication routing and protocol, which is more important if the system is made up of decentralized hardware agents. Generally in multi-agent problem solving, several agents work together to achieve a common goal. Due to their distributed nature, multi-agent systems can be more efficient, more robust, and more flexible than centralized problem solvers. On the other hand the type of communication among these hardware agents is an open problem, in which this paper presents an Evolvable Hardware (EHW) approach.

#### 1.1 Evolution of Communication

Different types of models for evolution of communication and language in artificial societies have been proposed. Cangelosi [Cangelosi 2001] with a distinction between signals, symbols and words has reported a simulation that shows the emergence of syntax and symbols from simple communication signals in population of foragers with neural network architecture for listener and speaker organisms to name foods. In a language game, Neubauer [Neubauer 2004] presents a simulation which shows the emergence of a communication system, with agents having communicative capabilities and the evolution of a language

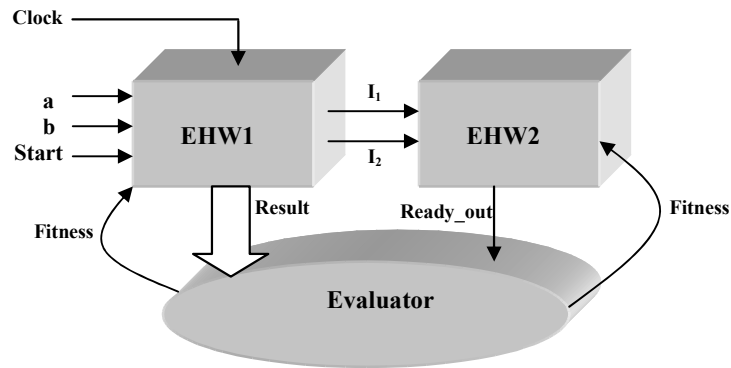
having a grammar. Using the mechanism of negotiation, developed in economics and game theory, Gmytrasiewicz et al [Gmytrasiewicz 2002] proposed another kind of evolution of an agent communication language. Thangavelautham et al [Thangavelautham 2003] used some agents without any centralized supervision that developed a communication protocol with a mutually agreed upon signaling scheme to share sensor data between a pair of individuals, for a lattice formation task. FSMs, neural networks [MacLennan 1999] and co-evolution [Yong 2001] has been previously used to emerge a kind of communication between agents. As an appropriate application, evolution of communication has been utilized in the community of robots to produce optimum communication code [Perlovsky 2005].

## 1.2 EHW

EHW is a new concept that targets the application of evolutionary algorithms to hardware design. EHW can adapt itself to unknown environment based on features of the reconfigurable hardware (e.g. FPGA). It uses genetic algorithm to search the goal architecture for hardware. The hardware architecture data is converted to chromosomes, where its fitness value will be derived in comparison with the target function, after the evolution process. As a good application one can refer to Thomson et al work [Thomson 2002], where a sequential digital filter with predetermined specifications is developed in an iterative process via automatically generated Verilog codes. To develop an EHW, one need to implement genetic algorithm as the evolutionary search engine in the target hardware. This has been well achieved by Gallagher et al [Gallagher 2004] using CGA architecture.

## 1.3 Getting All Together

After an introduction to evolution of communication in virtual environments (except the robots environment), we are interested to propose a new physical environment consisting EHW as the agents (which has been already discussed). Possessing the capability of reconfiguration with evolutionary optimization technique, EHW can be put to test to see if it can communicate with other EHW agents or not. In other words, the main goal of plan (that this work is the first step of it) is to evolve some peripheral cards (as a representation of EHW) to be able to communicate correctly with the motherboard in a small evolution time after they have been inserted in the slot. This system is supposed to result in evolution of the sender/receiver architecture and emergence of a protocol, i.e. an inter-EHW language. Finally optimum architecture and protocol are the secondary targets where, its problem solving without any supervision is a valuable outcome, especially when encountering faults in predesigned communications.



**Figure 1:** System diagram of an EHW-based, co-evolutionary serial-adder

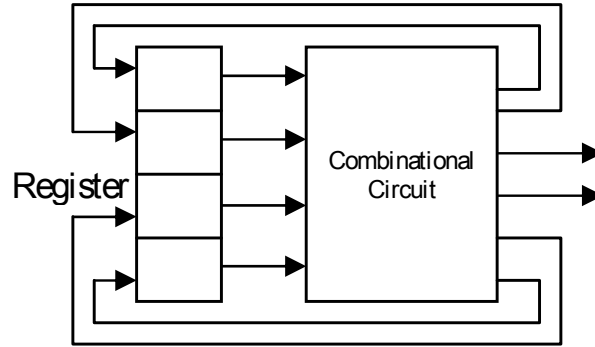
Consequently this way can be a fault tolerant approach too. This paper as the first step to the mentioned goals, shows the results of simulation of EHWs, trying to communicate to each other to achieve a goal and is organized as follows: Section 2 describes the overall system. Agents' details and their specifications are discussed in section 3. Simulation results are illustrated in section 4 and the paper concludes in section 5.

## 2 Outline

To test the possibility of self-organized communication for EHW with other reconfigurable agents, an experiment has been performed with the following parameters:

### 2.1 Goal and Architecture

As a sample of a sequential circuit, a serial adder is chosen to evolve. Its typical hardware description is centralized in one VHDL code [Navabi 1998], but in this work it is distributed into two agents. The only way for these two EHW cores to have the correct performance of a serial adder is to communicate with each other via their I/O ports. They should understand it themselves, to communicate. This is the goal of this simulation. For this purpose EHW1 is organized to perform arithmetic operations and EHW2 treats the only control output signal: ready-out. Figure 1 shows the overall diagram of the system, where communication ports are fixed between two agents. As Figure 1 shows, this is a one-way communication in which ready-out signal should be high, only the time that the



**Figure 2:** Representation of a sequential circuit

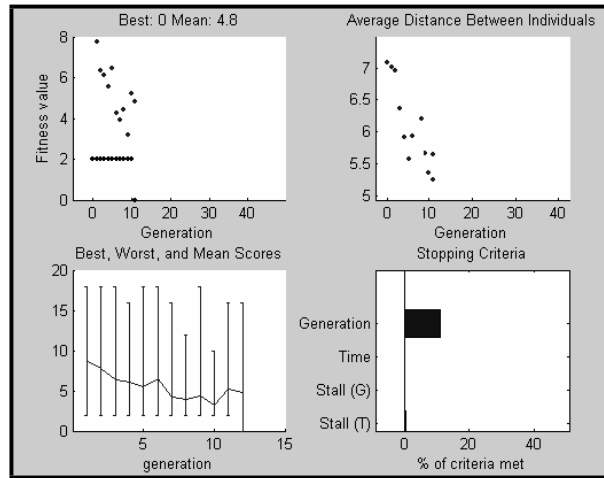
output of 8-bit serial adder is correctly available. The EHW1 has to make EHW2 aware of this stage with two accessible wires.

## 2.2 Evaluation Process

In the evaluation stage, the ready-out signal is multiplied by result output. The nonzero outcome that is not equal to  $a+b$ , and the zero signal 8 clocks after the start, increase the fitness, where zero product before 8 clocks (after start) and nonzero product that indicates  $a+b$  decrease the fitness. Using the mentioned fitness function, each of the EHWs has to adapt, to score the lowest, in an evolutionary process.

## 3 Agents' Specifications and Co-evolution

To score the best fitness, for either of the EHWs, they need a genetic optimizer, for reconfiguration. The most challenging stage is the representation process in which the hardware architecture should be coded into a chromosome chain. It is obvious from the nature of the problem, that the goal architecture is a sequential digital circuit. For an appropriate genotype, we used one of the standard forms of a sequential circuits (shown in Figure 2), in which, it is made up of an  $n$  bit register, and a combinational circuit that provides the feedback and outputs [Nelson 1995]. Using Figure 2, we only need to evolve the combinational circuit, for which, the truth table is used. The outputs columns of the truth table of the combinational circuit are used as the chromosome chain (the input columns are implicit) and a 4-bit register is roughly selected as a fixed parameter. Supposing 4 inputs for the truth table (as a result of a 4-bit register) and 6 outputs (4 register feedback as in Figure 2, and 2 I/O ports as in Figure 1), the sender (EHW1)



**Figure 3:** Representation of genetic algorithm process for EHWs

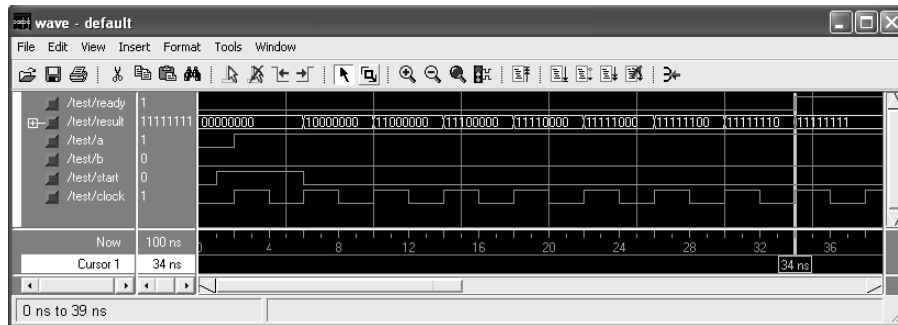
chromosome comes to  $24 \times 6 = 96$  chain bits. Not to complicate the EHW2, a 4-bit chromosome that stands for a 2 input/1 output combinational circuit (Figure 1) is supposed. A co-evolutionary process forms up, when EHW1 evolves to encode and EHW2 evolves to decode the signals, and they apparently affect each other when trying to hit the best fitness.

## 4 Simulation Results

### 4.1 Results

Each of the EHWs is equipped with an evolutionary search engine. In the genetic algorithm used in this experiment, a 30 individual population with two-point crossover and Gaussian function mutation operators, roulette selection mechanism and forward migration, met the lowest fitness (zero) in 11 generations. Figure 3 illustrates the evolution of generations in this simulation. After the evolution time (approximately 100 seconds), the system showed to work as well as a designed serial adder. Figure 4 shows how the system works. To ease the test, permanent signals of 1 and 0 are applied to a, b inputs respectively. 8 clocks (in the 9th rising edge) after the start signal, result output becomes 11111111, to show the sum of  $11111111 + 00000000$ . Ready signal rise exactly after the output is valid.

From the EHW point of view we are interested in what has happened between the two agents. This would be well presented by tracking the signals in the I/O ports between the two EHWs. These signals (I1,I2) are depicted in comparison with clock and ready signals in Figure 5. I1, I2 signals are made by the sender



**Figure 4:** The evolved serial adder, put to test

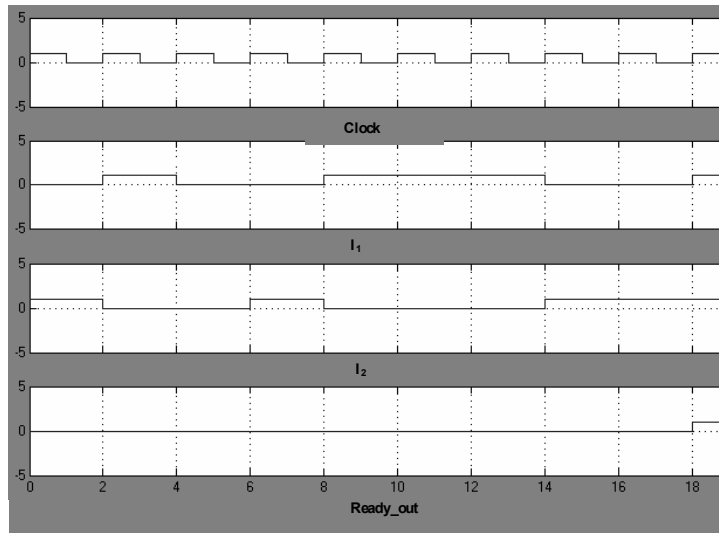
(EHW1) (see Figure 6) sequential circuit, where EHW2 (see Figure 6) made ready-out from the mentioned signals. Considering EHW2 4-bit chromosome chain [0 0 0 1], which is simultaneously its truth table, an AND gate seems to be evolved for the receiver circuit. Figure 5 clearly shows that: Ready-out = I1 AND I2.

## 4.2 Simulation Platform

EHW simulation, when using VHDL code to describe the agents, needs cooperation of a VHDL simulator with an evaluator and genetic software to determine the fitness and new chromosome, iteratively. For this purpose the Simulink, Genetic Algorithm and direct search and Link for ModelSim toolboxes of Matlab7.1 are utilized in cooperation with the Modelsim software in this experiment. The Simulink architecture of the EHWs is shown in Figure 7. The codes are then automatically generated for VHDL simulation in Modelsim.

## 5 Conclusion and Future Work

EHW as a new approach, instead of hardware design is considered as communicating agent. The performed simulation shows good results on capability of the sample EHW to recognize the need for communication in this case and make a simple protocol. Though solving the simple problem does not guarantee the generalization, it is an encouraging start. The next step is to analyze the evolved



**Figure 5:** The interface signals between the agents

$$\begin{aligned}
 \text{Evolved EHW1 Chromosome Chain} &= \left( \begin{array}{cccccc} 0 & 0 & 0 & 0 & 1 & 1 \\ 0 & 1 & 0 & 1 & 0 & 0 \\ 0 & 1 & 1 & 1 & 1 & 0 \\ 0 & 0 & 1 & 0 & 1 & 0 \\ 1 & 1 & 0 & 0 & 0 & 1 \\ 1 & 0 & 0 & 1 & 1 & 0 \\ 0 & 1 & 0 & 0 & 0 & 1 \\ 1 & 1 & 0 & 1 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 1 & 0 & 0 \\ 1 & 0 & 1 & 1 & 0 & 1 \\ 0 & 1 & 1 & 1 & 0 & 1 \\ 0 & 0 & 1 & 0 & 1 & 1 \\ 1 & 0 & 1 & 0 & 1 & 0 \\ 1 & 0 & 0 & 0 & 1 & 0 \\ 1 & 0 & 1 & 0 & 0 & 1 \end{array} \right) \\
 \text{Evolved EHW2 Chromosome Chain} &= \left( \begin{array}{c} 0 \\ 0 \\ 0 \\ 1 \end{array} \right) \\
 (1) & \qquad (2)
 \end{aligned}$$

**Figure 6:** The chromosome chain of evolved EHW1 and EHW2

protocol, even though it is usually harder than the hardware evolution process itself (like analyzing weights in a neural network). Another step from the future work list is the evolution of two-way communications for complicated tasks. We are hopeful that these researches pave the way for future adaptive hardware agents that no more need a common protocol, and can be leaved to make improvements, modifications and tolerate faults.

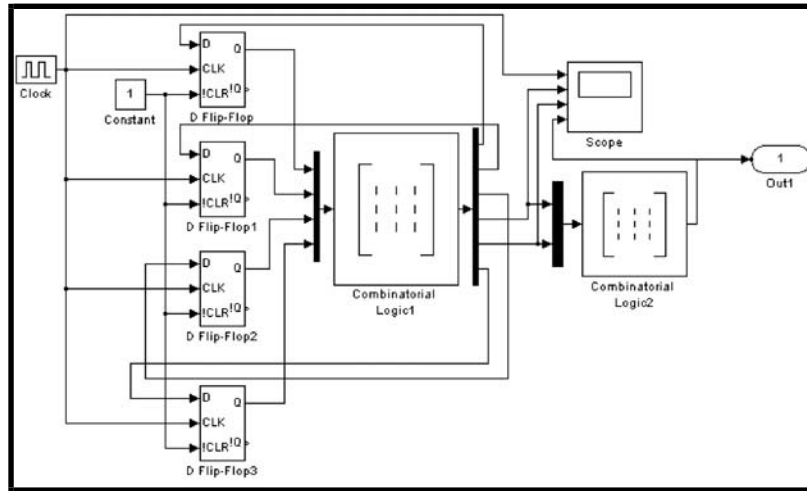


Figure 7: Simulink blocks of EHWs architecture

## References

- [Cangelosi 2001] Cangelosi A.: "Evolution of Communication and Language Using Signals, Symbols, and Words"; *IEEE Transactions on Evolutionary Computation*, 5, 2 (2001), 93-101
- [Neubauer 2004] Neubauer N.: "Emergence in a Multi-agent Simulation of Communicative Behavior"; *Publications of the Institute of Cognitive Science*, 11, (2004)
- [Gmytrasiewicz et al. 2002] Gmytrasiewicz J., Summers M., Gopal D.: "Toward Automated Evolution of Agent Communication Languages"; "Proceedings of the 35th Annual Hawaii International Conference on System Sciences (HICSS-35.02)", *IEEE* (2002)
- [Thangavelautham et al. 2003] Thangavelautham J., Barfoot D. T., Eleuterio G.: "Co-evolving Communication and Cooperation for Lattice Formation Tasks"; 7th European Conference on Artificial Life Dortmund, Germany, 14-17 Sept, 2003
- [MacLennan 1999] MacLennan B. J.: "The Emergence of Communication through Synthetic Evolution"; Technical Report UT-CS-99-431, 1999
- [Yong 2001] Yong C. H., Miikkulainen R.: "Cooperative Co-evolution of Multi-Agent Systems"; Technical Report AI01-287
- [Perlovsky 2005] Perlovsky L., Fontanari J.: "Evolution of Communication in a Community of Robots"; *IEEE Workshop on Advanced Robotics and Its Social Impacts*, (2005)
- [Thomson 2002] Thomson R., Arslan T.: "Evolvable Hardware for the Generation of Sequential Filter Circuits"; *Proceedings of the 2002 NASA/DOD Conference on Evolvable Hardware (EH'02)*, *IEEE* (2002)
- [Gallagher et al. 2004] Gallagher J., Vigraham S., Kramer G.: "A Family of Compact Genetic Algorithms for Intrinsic Evolvable Hardware"; *IEEE Transactions on Evolutionary Computation*, 8, 22(2004), 111-126



- [Navabi 1998] Navabi Z.: “VHDL, Analysis and Modeling of Digital Systems”; McGraw-Hill (1998)
- [Nelson 1995] Nelson V., Nagel H., Carrol B., Irwin D.: “Digital Logic Circuit Analysis and Design”; Prentice Hall (1995)